Differentially Driven Symmetric Microstrip Inductors

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Invited Paper

***Abstract*—A differentially excited symmetric inductor that enhances inductor quality (Q) factor on silicon RF ICs is presented. Compared with an equivalent single-ended configuration, experimental data demonstrate that the differential inductor offers a 50% greater Q factor and a broader range of operating frequencies. Predictions from full-wave simulations and a physics-based SPICE-compatible model are validated by experimental measurements on an inductor fabricated in a triple-level metal silicon technology. Application of the symmetric inductor to a cross-coupled oscillator improves output voltage swing and phase noise by 75% and 1.8 dB, respectively (for a given power consumption), while chip area is reduced by 35% compared to conventional inductor equivalents.**

***Index Terms*—Differential circuits, monolithic microstrip inductor, RFIC passive components.**

I. Introduction

MONOLITHIC inductors are an important component in highly integrated radio frequency circuits (RF ICs) for wireless communication systems such as personal communications services, wireless local area networks, satellite communications, and the global positioning system. External components are minimized when all passive components are integrated on-chip, so monolithic inductors are often used as narrow-band loads in RF circuits such as amplifiers, oscillators, and mixers. Through the use of on-chip tuned circuitry, a wide dynamic range may be preserved while using a relatively low supply voltage (i.e., 1–3 V).

The consumer electronics market favors silicon technology for its lower cost, higher yield, and the potential for combining analog and digital circuits. Silicon bipolar and BiCMOS technologies offer performance competitive with GaAs in the low-gigahertz frequency range. Nevertheless, monolithic inductors fabricated in production processes on medium resistivity substrates (i.e., $1\ \Omega \cdot \text{cm} < \rho < 15\ \Omega \cdot \text{cm}$) currently achieve a maximum quality (Q) factor on the order of 10 at low-gigahertz frequencies [1]–[4]. This poses a limitation for circuits such as LC oscillators, where phase noise is inversely proportional to the tank quality. The Q factor is constrained by conductor losses arising from metallization resistance, the conductive silicon substrate, and substrate parasitic capacitances (which lower the inductor self-resonant frequency). Several approaches have been used to improve the Q of monolithic inductors in silicon. These techniques include: lowering ohmic losses using thicker metallization [2], stacking of metal layers, and using lower resistivity metals (e.g., copper) [5]. Substrate losses have been reduced by fabricating the inductor on high-resistivity silicon ($\rho > 1\ \text{k}\Omega \cdot \text{cm}$) [6]–[8], or by selectively removing the underlying silicon substrate using a bulk micromachining technique (post-fabrication) [9]–[11]. A patterned ground shield has been demonstrated to be especially useful when attempting to realize an inductor on very low-resistivity substrates (i.e., $\rho < 0.1\ \Omega \cdot$ cm, [12]). Inductor chip area is reduced by connecting (overlaid) spiral inductors on multiple levels of metal in series, thereby increasing the inductance per unit area [13]. However, the Q factor is adversely affected by the nonuniform metal thickness in most VLSI technologies and increased interwinding and parasitic capacitances to the conductive substrate for multilevel spirals.

In this paper, we describe a symmetric inductor that is excited differentially (i.e., in the odd mode) to realize a substantially greater Q factor without altering the fabrication process [14]. It should be noted that differential circuits (amplifiers, mixers, and oscillators) are commonly used in monolithic transceiver designs because of their robustness and superior noise rejection properties (e.g., power supply noise rejection). A differential signal path typically requires twice the number of active and passive elements compared to a single-ended circuit; however, components can be added at little extra cost on an integrated circuit. This work shows that a symmetric inductor consumes less chip area as compared to single-ended equivalents when used in a typical circuit implementation.

II. Symmetric Inductors for Differential Circuits

A conventional spiral inductor and associated cross section are shown in Fig. 1. The inductor consists of a microstrip transmission line wound as a continuous metal spiral to reduce space. An underpass connects the inner node to other circuitry. In a differential circuit implementation, a pair of spiral inductors are used in the physical layout, as shown in Fig. 2(a). Although the overall circuit may be differential, the excitation of each inductor is "single-ended." That is, one terminal of the spiral is excited by an ac source while the other is connected to a common reference point (e.g., the supply voltage or ground). Note that

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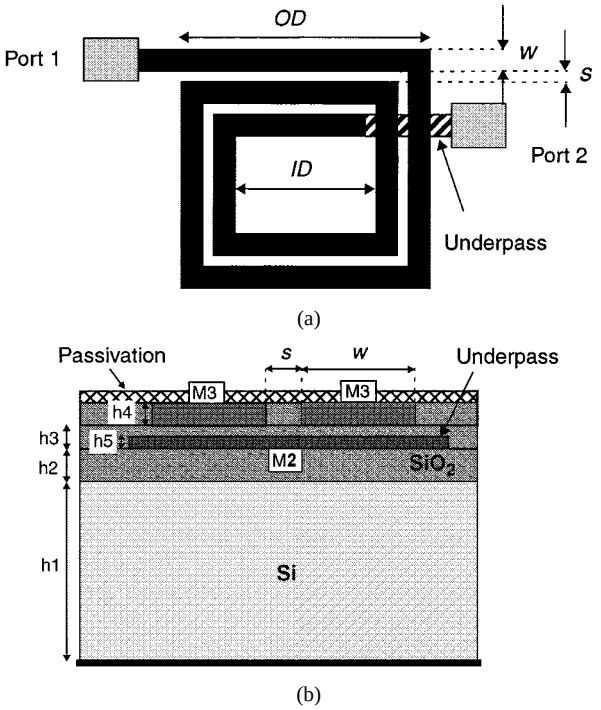


Fig. 1. Asymmetric microstrip spiral inductor. (a) Physical layout. (b) Cross section and fabrication parameters.

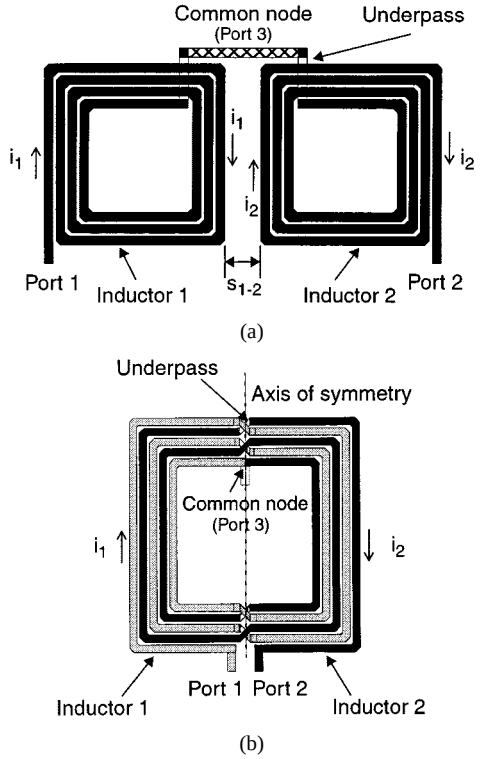


Fig. 2. Microstrip inductor physical layouts for differential drive. (a) Two asymmetric spiral conductors. (b) Symmetrical microstrip inductor.

signal currents associated with Ports 1 and 2 [i.e., i_1 and i_2 in Fig. 2(a)] flow in opposite directions and, hence, some physical separation (s_{12}) is required to limit the negative mutual magnetic coupling between the two inductors.

A. The Symmetric Inductor

The fully symmetric spiral inductor of Fig. 2(b) is *designed* for differential excitation (i.e., voltages and currents at Port 1 and Port 2 are 180° out of phase). When driven differentially, the voltages on adjacent conducting strips are anti-phase, however, current flows in the same direction along each adjacent conductor shown in Fig. 2(b) (i.e., signal currents i_1 and i_2 flow in the same direction on any side). This reinforces the magnetic field produced by the parallel groups of conductors and increases the overall inductance per unit area.

The symmetric microstrip inductor is realized by joining groups of coupled microstrips from one side of an axis of symmetry to the other using a number of cross-over and cross-under connections [see Fig. 2(b)]. This style of winding was first applied to monolithic transformers for coupling both primary and secondary coils by Rabjohn [15]. One advantage of a fully symmetric layout is that the two separate spirals are replaced by a single coil which has both electrical and geometric symmetry. This symmetry is important when locating the common node (a convenient bias point for active circuits), which separates the spiral into two inductances that have identical substrate parasitics at ports 1 and 2. As stated previously, a pair of asymmetric inductors must be spaced far enough apart to limit unwanted coupling (both magnetic and electric) between the inductor pair, which is not an issue for symmetric inductors. This is one of the reasons why a reduction in chip area results for the symmetric inductor. Also, the symmetric inductor is well suited for connection to active devices as the input ports (i.e., Ports 1 and 2) are on the same side of the structure.

B. Q Improvement by Differential Excitation

The monolithic inductor is a microstrip transmission line with an L/C ratio that favors inductance over capacitance. The Q factor improvement resulting from the differential drive can be estimated from the lumped-element equivalent circuit shown in Fig. 3(a) [7], [2]. This equivalent circuit accurately models the electrical behavior of the inductor up to the first resonance frequency. A simplified equivalent circuit for single-ended and differential excitation of the microstrip inductor are also shown in Fig. 3(b) and (c). Z_L is the impedance corresponding to the inductance and series dissipation (L and r), and Z_P is an equivalent shunt parasitic R–C network that has the same impedance as substrate parasitic elements C_{ox}, C_{si}, and R_{si} at a given frequency.

For single-ended excitation, the inductor is connected as a one-port as shown in Fig. 3(b). In this simplified equivalent circuit, the input impedance Z_{se} is a parallel combination of Z_L and Z_P, as indicated in the figure.

For differential excitation, the signal is applied between the two ports (Port 1 and Port 2) and the differential input impedance Z_d is the parallel combination of $2Z_P$ and Z_L. The substrate parasitics present a higher equivalent shunt impedance in the differential case and, therefore, Z_d approaches the value of Z_L over a wider range of frequencies than Z_{se}. At lower frequencies, the input impedance in either the shunt or the differential connections is approximately the same, but as the

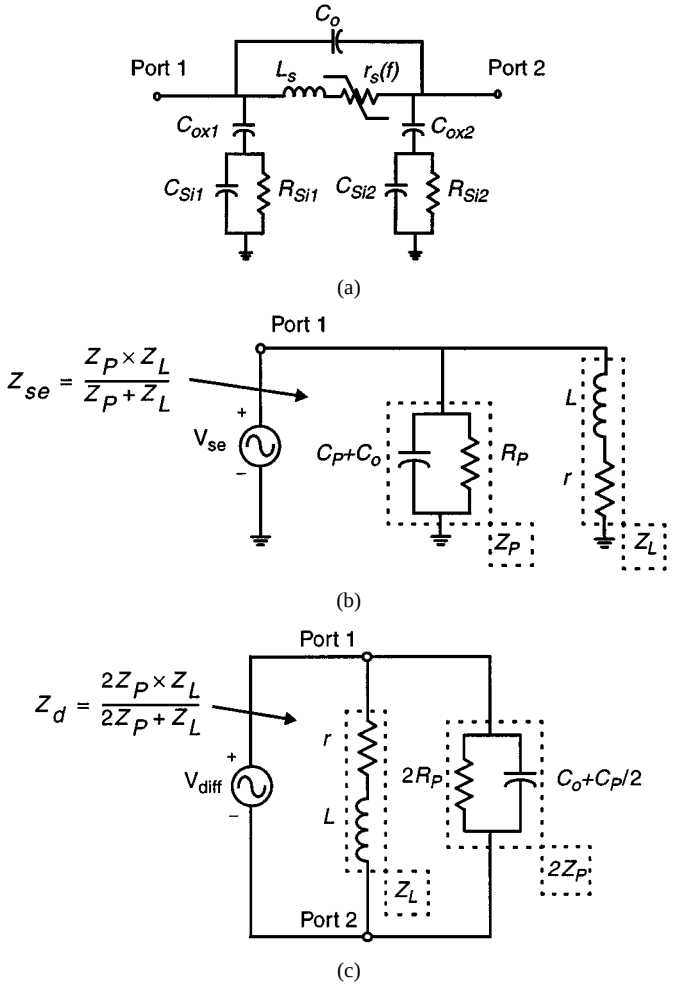


Fig. 3. (a) Lumped equivalent-circuit model of a microstrip inductor, and circuit equivalents for (b) single-ended (port 2 gounded) and (c) differential excitations.

frequency increases, substrate parasitics C_P and R_P come into play. For differential excitation, these parasitics have a higher impedance at a given frequency than in the single-ended connection. This reduces the real part and increases the reactive component of the input impedance. Therefore, the inductor Q is improved when driven differentially, and the self-resonant frequency (or usable bandwidth of the inductor) increases due to the reduction in the effective parasitic capacitance from $C_P + C_o$ to $C_P/2 + C_o$. The improvement in bandwidth was first noted for center-tapped spiral inductors in a monolithic bandpass filter application [16].

For these simplified model, the ratio of differential to single-ended Q factors is

$$\frac{Q_d}{Q_{se}} = \frac{2R_P \,||\, R_L}{R_P \,||\, R_L} \tag{1}$$

where $R_L = r(1 + Q_L^2)$ for $Q_L = \omega L/r$. At low frequencies, $R_P \gg R_L$ and the two Q factors are approximately the same. At lower frequencies, Q_L dominates in both cases and the Q factor increases for increasing frequency. At higher frequencies, R_L is increasing (as $Q_L \propto f$) and R_P is decreasing, so the differential Q factor becomes larger than the single-ended Q. Eventually, R_P dominates the inductor dissipation and the Q factor decreases with increasing frequency. The peak-Q occurs at a higher frequency when driven differentially due to the reduced effect of substrate parasitics in the differential case.

This analysis predicts Q improvement from differential excitation and that (ideally) the Q factor can be doubled in the differential connection [i.e., when $R_P \ll R_L$ in (1)] with no modifications in IC technology or processing.

It should be noted that this improvement in electrical performance is a property of differentially excited structures and that similar performance improvements could be expected from other transmission-line components such as: couplers, hybrids, and transformers, or even asymmetric inductors when excited differentially. The symmetric layout is useful to preserve the balance desired in the differential implementations most often used on RF ICs.

C. SPICE Model

For computer-aided design (CAD) purposes, a lumped-element equivalent or SPICE-compatible model is needed to predict the large-signal performance of an RF circuit correctly. Full-wave commercial electromagnetic simulators can be used to derive such models. However, these techniques generally require a great deal of CPU time and memory to simulate components with multiple metal layers and non-Manhattan physical layouts (such as the symmetric inductor). Therefore, simplified microstrip inductor CAD models that can be derived from layout and process fabrication parameters are required.

The modeling technique used here is applicable to any rectangular two- or three-port spiral inductor [17]. It uses closed-form expressions for the total inductance, resistance, and cross-under capacitance. A two-dimensional (2-D) quasi-static numerical method extracts the line capacitances, reducing computation time with minimal loss of accuracy for applications below approximately 10 GHz. The interwinding capacitances are obtained from the odd-mode mutual coupling of two coupled lines. The longitudinal component of the conduction current in a semiconducting substrate is included in the resistance model to account for all significant sources of loss. This method is numerically more efficient than full-wave modeling techniques and is sufficiently accurate for design purposes. The final inductor model is easily integrated into a circuit simulator, such as SPICE. In the following section of this paper, measurement and 3-D numerical simulation results are compared with this lumped-element model for the symmetric inductor.

III. Experimental Results and Discussion

In order to quantify the improvement in Q factor of the differentially driven symmetric design, a five-turn square symmetric spiral inductor (with nominal inductance of 8 nH) was designed and fabricated in a triple-level metal BiCMOS technology [18]. In this section, the experimental test structure is described along with the procedure used to extract the experimental data. Finally, the results are compared to theoretical predictions from full-wave and SPICE-compatible symmetric inductor models and other inductor designs reported in the recent literature.

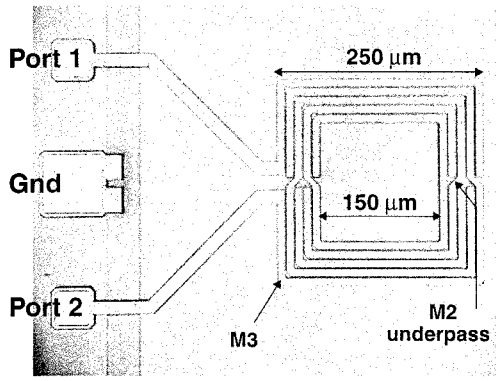


Fig. 4. Inductor test structure.

TABLE I
SUBSTRATE AND METAL PARAMETERS FOR THE BiCMOS TECHNOLOGY

Parameter	Value
Oxide thickness over M2, h3 - h6	1.3 μm
Oxide thickness below M2, h2	3.61 μm
Silicon resistivity	15 Ω-cm
Silicon thickness, h1	200 μm
Metal resistivity	31 mΩ-μm
M3 thickness, h4	2.07 μm
M2 thickness, h5	0.84 μm

A. Symmetric Inductor Test Structure

The symmetric inductor test structure, including signal-ground-signal testpads is shown in Fig. 4. The outer dimension, OD, is 250 μm, the top conductor ($\mathrm{M3}$) microstrip line is 8 μm wide, and the spacing (s) between conductors is 2.8 μm. The void between opposite groups of coupled lines (ID) is approximately 150 μm, which results in negligible negative mutual coupling between coupled-line groups. The relatively narrow conductor width and spacing results in higher positive magnetic coupling on any one side and lower substrate capacitive parasitics. Second-level metal ($\mathrm{M2}$) is used for the metal underpasses. Both signal and ground pads are located on the same side; thus a set of probes with two adjacent RF contacts was used for testing. Properties of the substrate and the aluminum metallization for the fabrication process are listed in Table I. For Y–Z parameter deembedding purposes [19], short and open test structures or "dummies" were also fabricated.

B. Differential s-Parameters and Input Impedance

Single-ended and differential configurations are derived from the two-port measurements, as shown in Fig. 5. The s-parameters are given by

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3}$$

where $a_k = E_{ik}/\sqrt{Z_o}$ and $b_k = E_{rk}/\sqrt{Z_o}$ with $k = 1, 2$. E_i and E_r are the incident and reflected voltage waves, respectively, and Z_o is the system impedance (typically 50 Ω). The difference between equations (2) and (3) gives the reflected differential signal, E_{rdiff} (i.e., $E_{\mathrm{rdiff}} = b_1 - b_2$). For a pure difference mode signal, $E_{i1} + E_{i2} = 0$ or $a_1 = -a_2 = a$. Therefore, for an incident signal $a = E_i/2\sqrt{Z_o}$, the differential one-port s-parameter S_d, can be written in terms of the single-ended S-parameters as

$$S_d = \frac{b_1 + b_2}{2a} = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2} \tag{4}$$

and the corresponding input impedance is

$$Z_d = 2Z_o\left(\frac{1 + S_d}{1 - S_d}\right) \tag{5}$$

where $2Z_o$ is the differential system impedance.

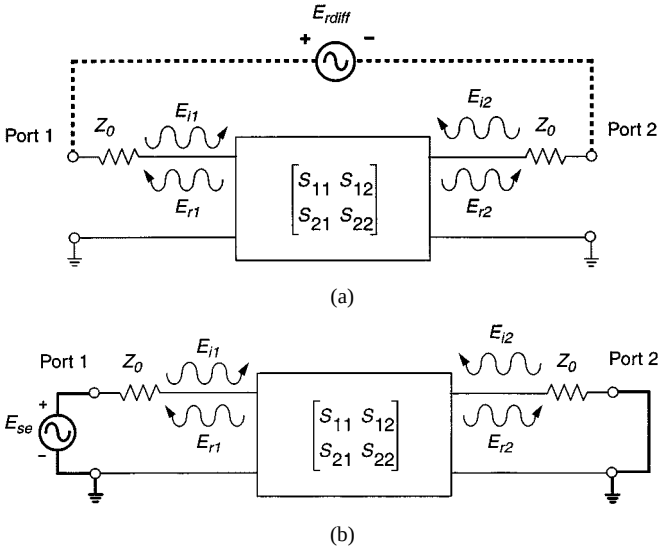


Fig. 5. Two-port in differential and single-ended configurations. (a) Differential connection. (b) Single-ended connection.

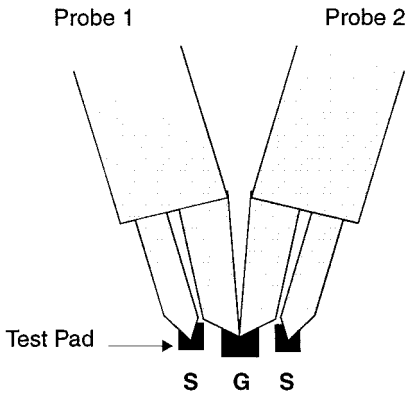


Fig. 6. Signal–ground–signal (SGS) probe configuration for measurement.

C. Measurement Procedure

The symmetric inductor was characterized experimentally from on-wafer measurements using a two-port vector network analyzer and coaxial RF probes. The probes configuration consists of two signal-ground coaxial 50-Ω probes mounted on a single base, as shown in Fig. 6. A spacing of 150 μm between the ground (G) and signal (S) fingers was used.

Signal–ground short, open, load, and thru impedance standards were used to perform a full SOLT two-port calibration.

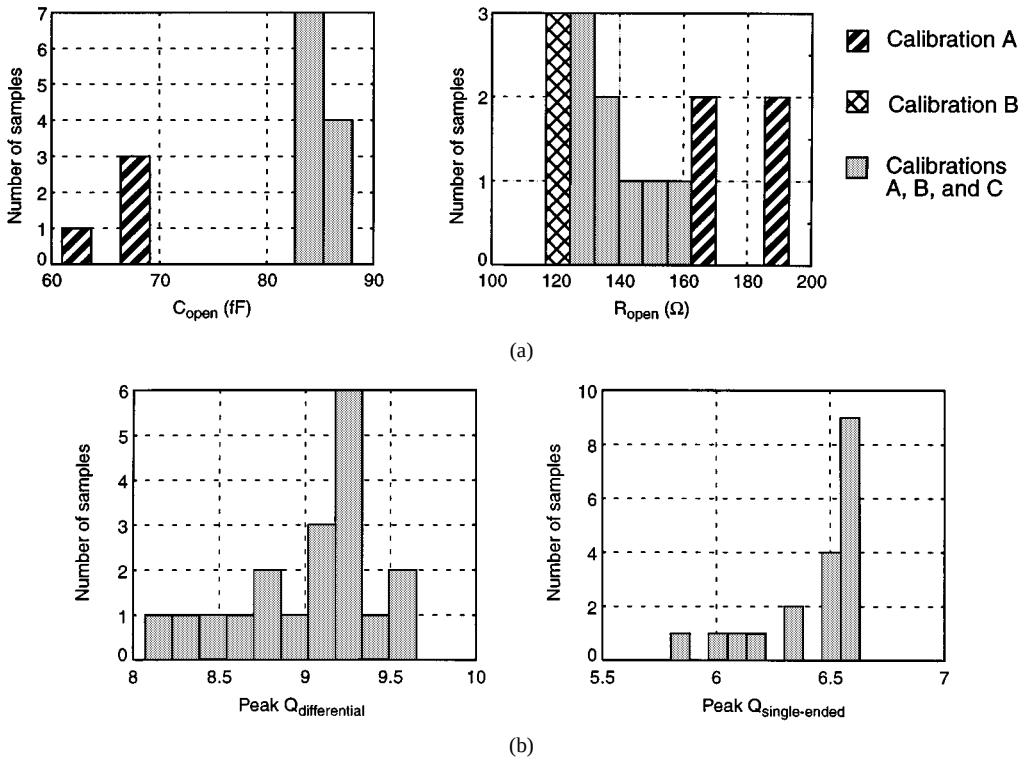


Fig. 7. Histograms from experimental measurement of the 8-nH test inductor. (a) Open dummy structure parasitic histograms over 15 samples. (b) Q factor histograms over 19 samples.

During calibration, Probe 2 of the set of dual probes is mounted on a manipulator opposite to Probe 1. After calibration, Probe 2 is moved back to the same probe head as Probe 1 so that the probes appear as shown in Fig. 6. Moving one probe between calibration and measurement steps can introduce errors into the measurements due to phase instability of the cable. This error was minimized through the use of flexible cables with high phase stability and a verification check of the calibration with the probes in the final configuration.

Measurements were deembedded by: 1) measuring single-ended two-port s-parameters of the inductor test structure; 2) measuring the open dummy structure and deembedding the shunt parasitics through y-parameter subtraction; and 3) measuring the short dummy structure and deembedding the series parasitics through z-parameter subtraction [19]. The probe contact resistance is approximately 0.25 Ω for the first touchdown and can increase significantly after repeated touchdowns due to contact wear of both the probe and testpad. Therefore, measurement of the contact resistance by probing the short deembedding structure is important to obtain consistent measurements.

D. Measurement Results

The interconnections of the short deembedding structure can be modeled as a 250-pH inductance in series with a 0.1–0.4-Ω frequency-dependent resistance, as determined from measurement (after accounting for a probe contact resistance of 0.3 Ω). These measurements are consistent with the values determined from full-wave numerical simulations (220 pH in series with 0.25 Ω). Shunt parasitic values at 2 GHz for the open structure are shown as histograms in Fig. 7(a). Depending on the calibration, different values were obtained. However, the relatively small pad parasitics only affect the inductor behavior near the self-resonant frequency.

Fig. 7(b) shows the Q factors (single-ended, Q_{se} and differential, Q_d) computed from the deembedding s-parameter measurements on 19 samples. The peak Q value for each measured sample is shown in the figure. The Q factors of 9.3 and 6.6 for Q_d and Q_{se}, respectively, occurred with the greatest probability (30%–50%). For subsequent discussions, a representative sample from these measurements is shown.

A comparison between the experimental measurements, full-wave EM simulation, and the lumped-element (SPICE) inductor model for the input impedance and the Q factor are shown in Figs. 8 and 9. Good agreement is seen between measurement and simulation. At lower frequencies, the difference in Q between the differential and single-ended excitations is not significant ($<$1%) because the shunt capacitive parasitic components do not affect the low-frequency input impedance. Hence, the two cases can be represented by a series L–r model. However, as the frequency increases, the difference between the input impedances (see Fig. 8) becomes substantial; Z_d is much lower than Z_{se} by an increasing factor. This is caused by the lower effective substrate parasitics present in the differentially excited case. The difference between the Q factors in the differential and single-ended cases (Fig. 9) illustrates this point. The peak in the Q factor is a result of the shunt parasitics as previously described. Lower parasitics for differential excitation result in a higher peak Q factor and broadening of the Q peak compared with the single-ended (conventional) connection.

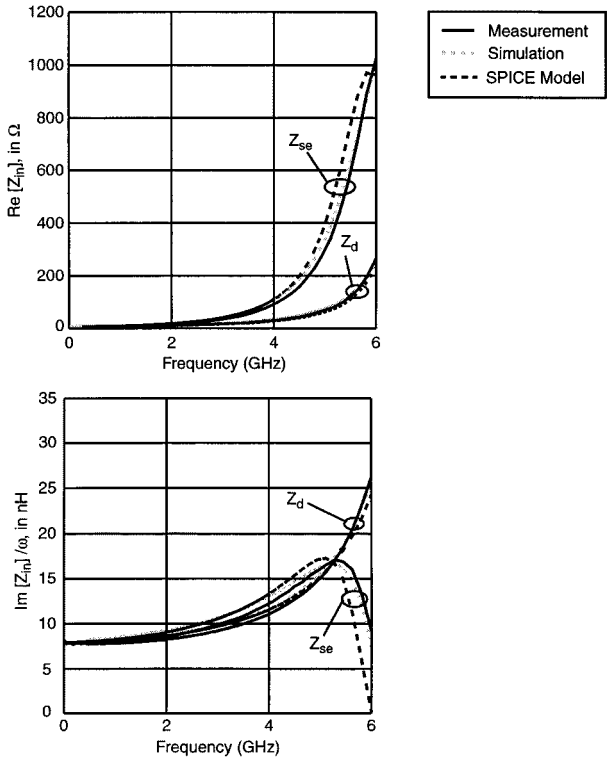


Fig. 8. Measured and simulated resistive and inductive parts of the input impedance for single-ended and differential connections.

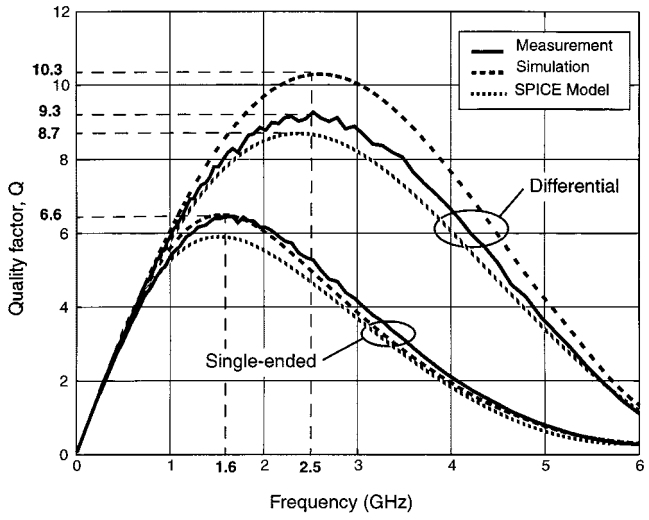


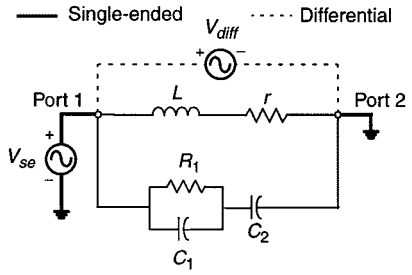
Fig. 9. Measured and simulated Q factors for single-ended and differential excitations.

Table II compares the corresponding peak Qs for the single-ended and differential excitation cases. Due to a lower series resistance and a higher inductance, the simulated data have the highest Q factor. The peak Q occurs at frequencies of 1.6 and 2.5 GHz for the single-ended and differential excitations, respectively. Thus, a higher Q factor at a higher operating frequency is observed, as predicted previously. Note that this improvement in Q is achieved without any modification to the fabrication process. Achieving a comparable Q value in the single-ended connection would require approximately a twofold increase in the top metal thickness (e.g., increasing topmetal thickness from 2 to 4 μm would result in a single-ended Q of 8.5 at 2.2 GHz, from simulation). At frequencies beyond the Q-peak, an increase of greater than 50% can be achieved. It should be noted that because they are greater in magnitude, Q values for the differential case are much more sensitive to slight variations in the measured or simulated input impedance. Thus, near the peak Q for the differential case, the relative effect of an error in either the measurement or simulation is more pronounced. Because of lower capacitive parasitics, the inductor self-resonance is increased from 6.3 GHz for the single-ended case, to 7.1 GHz for the differential excitation, implying a broader useful bandwidth for differentially excited inductors.

Fig. 10 shows a simplified lumped-element model for the symmetric inductor that was fit numerically over a broad band of frequencies (0.5–6 GHz) for both the single-ended and dif-

TABLE II
PEAK Q-FACTOR FOR SINGLE-ENDED AND DIFFERENTIAL EXCITATIONS

Results	Q_{se} (1.6 GHz)	Q_d (2.5 GHz)	% increase
Measurement	6.6	9.3	41%
Simulation	6.6	10.3	56%
Model	5.9	8.7	47%



equivalent circuit model for parameter extraction.

L and r values.

Elements	Measured	MoM Sim.	SPICE Model
L, in nH	7.8	8.3	8
r, in Ω	7.8	8.2	7.7

Substrate parasitics for single-ended and differential excitations.

	Elements	Single-ended	Differential	Diff/S-E Ratio*
Measurement	R_1, in Ω	358	1000	2.8 times
	C_1, in fF	135	85	53%
	C_2, in fF	162	75	46%
MoM Sim.	R_1, in Ω	358	1000	2.8 times
	C_1, in fF	135	95	70%
	C_2, in fF	162	62	38%
SPICE Model	R_1, in Ω	500	1200	2.4 times
	C_1, in fF	135	80	59%
	C_2, in fF	210	80	38%

* Ratio of differential to single-ended component values

Fig. 10. Extracted values of equivalent circuit parameters for single-ended and differential excitations.

TABLE III
INDUCTOR COMPARISON

Inductor type	Reference	ρ_{sub} (Ω-cm)	t_M (μm)	L (nH)	Q_{peak}
1-level metal	Long [2]	10	1-3	1.88	6-10 @ 4 GHz
2 stacked metals	Park [8]	2 k	2	13	12 @ 3 GHz
3 stacked metals	Burghartz [5]	12	4.3	2.2	16 @ 2 GHz
Ground shield	Yue [12]	10-20	2	8	7.2 @ 1.5 GHz
Membrane	Chi [10]	2 k	1 (Au)	0.9 1.2	20 @ 4.3 GHz f_{sr}: 70 GHz
Etched oxide/Si	Rieh [21]	10 k		2	f_{sr}: 30 GHz
Differential Single-ended	this work	15	2	8	9.3 @ 2.5 GHz 6.6 @ 1.6 GHz

ferential connections. The tables in the figure list the element values for measured and simulated results. Here, L is the low-frequency inductance, and r is the series resistance at 500 MHz. As shown in Fig. 10, the resistive element of the shunt parasitics is more than twice as high when both single-ended and differential equivalent parameter values are compared, and the shunt capacitances are 40%–60% of those in the single-ended case, which verifies the predictions made from the simplified lumped-element model in Section II-B. Reasonably good agreement is seen between SPICE model, MoM simulation, and experimental measurements.

E. Sources of Error

Calibration, deembedding structure parasitics, and probe contact resistance are all sources of error that can alter the measured data. Inaccuracies due to imperfections in the connectors, cables, temperature and frequency drifts within the network analyzer, calibration, and test devices also add to the random measurement errors [20].

Other errors are caused by variations in the fabrication process. An important factor is the top metal thickness, which can vary by $\pm$10%. A 10% increase in the metal thickness reduces R_{dc} to 6.8 Ω, and the simulated series resistance becomes 7.6 Ω at 500 MHz, compared with the measured value of 7.7 Ω. In a submicrometer IC technology, the metal lines are defined photolithographically to within 0.1 μm and, therefore, variations in processing have a negligible effect on the line inductance and resistance as these parameters are defined primarily by the conductor width and spacing. Simulations were performed for a $\pm$0.2 μm strip width variation, and no significant changes ($<$2% in the peak Q) were observed. For a $\pm$1-μm change in oxide thickness and a $\pm$50% change in silicon resistivity, simulations also predict a $\pm$5% variation in the self-resonant frequency and in the peak Q.

Inaccuracies in full-wave simulation are mainly caused by improper meshing of the structure and inaccurate compensation for finite metal thickness, as conductors of infinitesimal thickness are assumed by the method-of-moments (MoM) algorithm. It should also be noted that present simulators do not account for variations in temperature of the metal in a spiral inductor.

F. Literature Comparison

In Table III, the symmetric spiral inductor is compared with other Q improvement techniques. Simple planar spirals with single and stacked metal layers are represented. Note that the Q factor generally improves for smaller inductor values within any given technology or design technique. Higher Q is realized by either increasing metal thickness (through metal stacking or thicker conductors) or by reducing losses in the substrate. Substrate losses are reduced dramatically when the inductor is fabricated on semi-insulating material, however, this in incompatible with current active device technology. Substrate removal (as in the membrane or etched oxide designs) or a ground-shielded design are the other options for limiting substrate losses. The performance of the differentially driven symmetric inductor is competitive with many of these other designs. It should also be noted that differential drive of the inductor can be implemented in all of the aforementioned technologies to further enhance the overall Q and obtain broader operating bandwidth.

IV. APPLICATIONS EXAMPLE

This section uses a common RF IC application of monolithic inductors to illustrate the advantages of the symmetric design over the integration of two identical asymmetric inductors. Here, the 8-nH symmetric inductor is incorporated into an oscillator designed for the 2.4–2.48-GHz ISM band. The oscillator circuit of Fig. 11 uses two transistors in a fully differential, cross-coupled configuration. A differential implementation has the advantages of common-mode power supply noise rejection, lower harmonic generation, and higher output voltage swing at the expense of greater power consumption and chip area. The intermediate frequency (IF) for this application is specified at around 350 MHz and therefore a local oscillator frequency of 2.05 to 2.1 GHz is required. For a resonance to occur at 2.1 GHz, the combined capacitance across inductance L_1 due to lumped capacitances C_1–C_3 and device parasitics should be approximately 0.72 pF. Bias resistors R_1 and R_2 are made large to isolate the bias network from the RF signal path.

The performance of the cross-coupled oscillator was compared for symmetric and asymmetric inductors in the tank

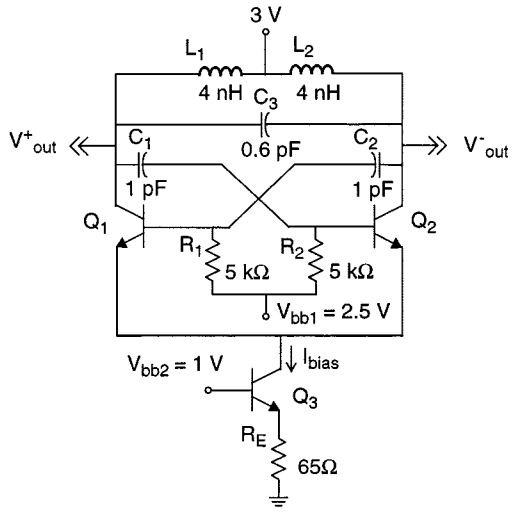


Fig. 11. Cross-coupled oscillator circuit.

TABLE IV
COMPARISONS BETWEEN 8-nH SYMMETRIC AND 4-nH CONVENTIONAL INDUCTORS

Characteristics	8 nH symmetric	4 nH asymmetric
OD / No. of turns	250 μm / 5	210 μm / 3.5
Inner gap, ID	150 μm	140 μm
Unwound length	4 mm	2.44 mm
R_{dc}	7.5 Ω	4.56 Ω
Q @ 2.1 GHz	8.6	7.5

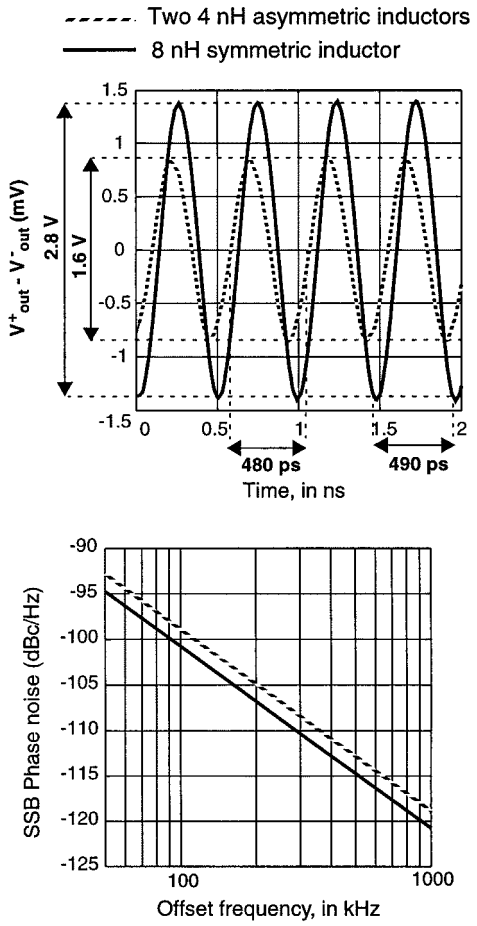


Fig. 12. Differential output voltage oscillation and phase noise for the 8-nH symmetric inductor and two 4-nH asymmetric spiral inductors.

circuit (with physical layouts of the inductor styles as in Fig. 2). One design incorporates two 4-nH conventional (i.e., asymmetric) spiral inductors, while the other employs a single 8-nH symmetric inductor. Characteristics of the asymmetric 4-nH spirals and the 8-nH symmetric inductor are listed in Table IV. The technology parameters of Table I were assumed for both inductors. Also, the distance between the two 4 nH adjacent spirals is assumed to be much greater than the spacing listed in the Table ($s_{12} = 40$ μm) so that electromagnetic coupling between inductors is minimized. Note that as a load for the cross-coupled oscillator, the 8-nH symmetric inductor is excited differentially whereas the two 4-nH conventional spirals are each connected in the single-ended configuration. Fig. 12 shows the differential output voltage and the single-sideband phase noise for electrical simulations of the differential oscillator for both inductor configurations. Table V compares the performance of the oscillator for each inductor configuration. Due to the lower tank impedance at resonance and Q factor for the conventional spiral compared to the symmetric spiral inductor, a lower output swing and a poorer phase noise result. However, the phase noise of the two-inductor design could be improved at the expense of increased bias current. Simulations using compact models for the inductors rather than s-parameter data symmetric inductors compare within 3% for the overall oscillator performances.

TABLE V
COMPARISON OF CROSS-COUPLED OSCILLATOR PERFORMANCE FOR BOTH INDUCTORS

Parameters	8 nH symmetric	4 nH asymmetric
f_{osc}, in GHz	2.061	2.114
V_{out}, in V	2.8	1.6
Phase noise (dBc/Hz) @ 1 MHz offset	-120.7	-118.9
P_{out}, in dBm	7.1	5.4
3rd harmonic P_{out}, in dBm	-30.9	-29.1

Chip area is an important design issue as it relates directly to the component cost in production. The symmetric inductor reduces the total area by 35% when compared with two 4-nH conventional inductors with a 40-μm spacing. Therefore, the differential oscillator using a single symmetric inductor realizes a substantial reduction in the overall chip area as well as improved electrical performance [17]. These benefits have also been demonstrated in other applications of monolithic microstrip components and differential circuits on RF ICs [22]–[24]. The main disadvantage of these components is the increased design time compared to asymmetric inductors, as simulation time and memory requirements are related to the complexity of the physical layout.

V. Conclusion

A symmetric inductor structure which is excited differentially and realizes a substantial improvement in both Q factor and component bandwidth was presented. Differentially excited inductors are less affected by substrate parasitics, which was demonstrated from both simulation and measurement. This leads to higher Q factors than for a single-ended equivalent when fabricated in silicon technology, where losses in the semiconducting substrate affect the component Q. In addition, a single symmetric inductor replaces two conventional (asymmetric) spirals to reduce chip area as well as improve electrical performance.

It was shown that the peak Q factor of a five-turn 8-nH inductor increases by 50% and that a broader operating bandwidth is achieved when differentially excited. This improvement in Q factor translated directly into lower phase noise and greater output signal swing (at a given power consumption) for the oscillator example presented in this paper. The experimental Q factor measurements were confirmed by full-wave and lumped-element (SPICE-type) model simulations.

It should be noted that this improvement in electrical performance is a property of differentially excited structures, and similar performance improvements are expected from passive devices such as couplers, hybrids, and transformers when excited differentially. A symmetric layout is useful to preserve the balance desired in differential implementations most often used on RF ICs.

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